REMARKS

The Office Action mailed October 23, 2002, has been received and reviewed. Claims 3 through 22 are currently pending in the application. All claims stand rejected. No claims have been amended by way of the present communication. Applicants respectfully request reconsideration of the application in view of the following remarks.

Information Disclosure Statement

Applicants note the filing of an Information Disclosure Statement herein on July 12, 2000 and note that no copy of the PTO-1449 was returned with the outstanding Office Action. Applicants respectfully request that the information cited on the PTO-1449 (which is the same as that of record to date in the parent application hereto) be made of record herein.

35 U.S.C. § 103(a) Obviousness Rejections

(A) Applicable Authority

The basic requirements of a *prima facie* case of obviousness are summarized in MPEP §2143 through §2143.03. Section 2143 states:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success [in combining the references]. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Further, in establishing a *prima facie* case of obviousness, the initial burden is placed on the Examiner. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the

claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). *See also*, MPEP §706.02 (j) and §2142.

(B) Obviousness Rejection Based on U.S. Patent 5,428,244 to Segawa et al. in view of U.S. Patent 5,438,006 to Chang and further in view of U.S. Patent 4,704,783 to Possin et al.

Claims 3 through 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,428,244 to Segawa et al. (hereinafter the "Segawa reference") in view of U.S. Patent 5,438,006 to Chang (hereinafter the "Chang reference") and further in view of U.S. Patent 4,704,783 to Possin et al. (hereinafter the "Possin reference"). As the Examiner has failed to establish a *prima facie* case of obviousness based upon the asserted combination of references, Applicants respectfully traverse this rejection, as hereinafter set forth.

For the sake of convenience, the independent claims to which the § 103(a) rejection applies are summarized herein. Independent claim 3 recites a method of forming a gate stack. The method comprises forming a gate dielectric layer on a silicon substrate, forming a polysilicon layer on top of the gate dielectric layer, subjecting the polysilicon layer to an ion implantation of impurities, depositing a metallic silicide film in a non-annealed state atop the polysilicon layer and depositing a dielectric cap layer over the metallic silicide film *at a temperature below about 600°C.*

Independent claim 17 recites a method for forming a gate stack comprising providing a semiconductor substrate with a dielectric layer on an active surface of the semiconductor substrate, wherein a polysilicon layer is disposed over the dielectric layer. The method further comprises forming a metallic silicide film in a non-annealed state over the polysilicon layer; forming a dielectric cap on the metallic silicide film *at a sufficiently low temperature that the metallic silicide film remains in the non-annealed state*; forming and patterning a resist layer on the dielectric cap; etching the dielectric cap, the metallic silicide film and the polysilicon layer; and stripping the resist layer. The Specification of the present invention clearly indicates that a metallic silicide film may be annealed to form a crystalline structured metallic silicide film and

that such annealing causes the silicon within the metallic silicide to form clusters inside the crystalline structured metallic silicide film. *See, Specification* at page 5, lines 11–24. Further, it is stated that the formation of silicon clusters within the metallic silicide film may be caused if the dielectric cap is formed at a temperature of 600°C or more. *Id.* Thus, in order for the metallic silicide film to remain in the non-annealed state, and thus prevent the formation of silicon clusters within the metallic silicide film, a "sufficiently low temperature" as recited in independent claim 17 is one that is below about 600°C.

Independent claim 19 recites a method of forming a gate stack consisting essentially of forming a gate dielectric layer on a silicon substrate, forming a polysilicon layer on top of the gate dielectric layer, subjecting the polysilicon layer to an ion implantation of impurities, depositing a metallic silicide film in a non-annealed state atop the polysilicon layer, and depositing a dielectric cap layer over the metallic silicide film *at a temperature below about 600°C such that the metallic silicide film remains in the non-annealed state.*

It is respectfully submitted that a *prima facie* case of obviousness cannot be established based upon the asserted combination of references as there is no "suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the [Segawa and Chang] reference[s]" with the method of the Possin reference as asserted in the outstanding Office Action. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The Segawa reference discloses a number of methods for promoting adhesion between a metallic silicide film and an overlaying dielectric layer and for decreasing peeling during subsequent heat treatments. The methods include forming a metallic silicide layer and silicon-rich dielectric cap during the formation of a gate stack structure. The silicon-rich dielectric cap has a silicon-to-other element (*e.g.*, oxygen or nitrogen) ratio that includes a silicon content that is higher than the silicon-to-other element ratio according to the stoichiometric composition of the formula of the deposited material (*e.g.*, SiO_2 or SiN_3). *See, Segawa reference* at col. 1, lines 10-13; col. 3, lines 49-53. In each instance disclosed by the Segawa reference, the temperature used during the formation of the silicon-rich dielectric cap over a metallic silicide film exceeds 600°C. More specifically, the temperatures disclosed by the Segawa reference for the formation

of a silicon-rich dielectric cap over a metallic silicide film are a temperature of 840°C (Examples I and II), a temperature of 760°C (Examples III and IV), a temperature of 850°C (Examples V and VI) and a temperature range of 650°C to 700°C (Examples VII and VIII). The Segawa reference states that the disclosed reaction chamber process parameters, including the delineated temperature parameters, result in a dielectric cap having the desired properties (*i.e.*, a silicon-to-other element ratio in excess of the silicon-to-other element ratio of the stoichiometric composition of the material deposited). *See id.* at col. 7, lines 40-48; col. 9, lines 10-14; col. 10, lines 9-14; col. 11, lines 7-13. This silicon-to-other element ratio is desired as it permits gate impurities diffused from below the dielectric layer to be bonded to silicon with no chemical bond to oxygen and with vacancies for further chemical bonding. Consequently, the concentration of gate impurity scattering the interface is decreased which improves adhesion between the metallic silicide film and the dielectric layer and, thus, decreases peeling during subsequent heat treatments. *See id.* at col. 8, lines 1-16.

According to the findings disclosed in the Specification of the present application, each of the temperatures for forming a dielectric cap over a metallic silicide layer disclosed by the Segawa reference is likely to result in the formation of silicon clusters within the metallic silicide film because the temperatures exceed 600°C. *See, Specification* at page 5, lines 11-24. The use of such temperatures to form a dielectric cap over a metallic silicide film is undesirable if one also wishes to prevent the pitting of the gate dielectric layer and/or silicon substrate during gate stack formation. *See, Specification* at page 5, line 25 – page 6, line 2.

That the Segawa reference does not teach or suggest a method for forming a dielectric cap layer at a temperature below about 600°C is acknowledged by the Examiner at page 4, ¶ 2 of the outstanding Office Action. However, there is an inconsistency in the outstanding Office Action between this acknowledgement and a description of Example VII of the Segawa reference provided at page 3, lines 2-9 wherein it is stated that the silicon oxide layer and tungsten silicide layer "have the same deposition temperature." This assetion is based upon the unsupported statement that "since both the silicon oxide layer and tungsten silicide layer are formed from the SH_2Cl_2 gas, the two layers have the same deposition temperature." *See, Office Action* at page 3, lines 6-8. It is respectfully submitted that the disclosure of the Segawa

reference does not support this allegation. Nowhere in the disclosure of the Segawa reference is there any indication that using SH_2Cl_2 gas to deposit both the tungsten silicide and silicon oxide layers produces equivalent deposition temperatures. In fact, the Segawa reference specifically teaches that the deposition temperature used to form the dielectric cap layer is higher than the deposition temperature used to form the metallic silicide layer. The difference in the temperatures is confirmed by the statement that the two layers have "**almost** the same deposition temperature." *See, Segawa reference* at col. 14, lines 7-8 (emphasis added). The inclusion of the term "almost" in the example of the Segawa reference directly opposes the allegation of the outstanding Office Action that the deposition temperatures disclosed by the Segawa reference are the same for the metallic silicide film and the dielectric cap layer.

Furthermore, the disclosure of the Segawa reference specifically teaches that the deposition temperature of the tungsten silicide film and the silicon oxide layer are not the same. Even though a flow of SH_2Cl_2 gas to the CVD reaction chamber in Example VII of the Segawa reference is kept at a constant rate, the temperature within the reaction chamber is raised between the deposition of the tungsten silicide film and the deposition of the silicon oxide film. Specifically, "(1) the supply of WF_6 gas is brought to a halt, (2) at the same time, the chamber temperature is increased up to 650°C to 700°C, and (3) N_2O gas is introduced into the chamber at a flow rate of 0.4 to 0.6 lit. per minute (from t2 in FIG. 13)." *See, Segawa reference* at col. 13, lines 55-59. The introduction of the N_2O gas, which initiates and is required for the deposition of the silicon oxide, does not occur until after the temperature within the deposition chamber is raised above 600°C, specifically to a temperature between 650°C and 700°C. The fact that the temperature is above 600°C for the deposition of the silicon oxide layer is further supported by FIG. 13 of the Segawa reference. FIG. 13 clearly shows that prior to the time that the WF_6 flow ceases (time t1), the temperature is being raised within the deposition chamber. At the time the flow of N_2O is initiated (time t2), the temperature is already well above 600°C. Because N_2O must be present for the deposition of the silicon oxide, the earliest time at which the deposition of the dielectric layer of the Segawa reference can begin is time t2. At time t2, the temperature in the deposition chamber is above 600°C as disclosed by Example VII and illustrated in FIG. 13.

In light of the above, Applicants respectfully submit that the acknowledgement at page 4, ¶2 of the outstanding Office Action that the Segawa reference does not teach or suggest a method of depositing a dielectric cap layer at a temperature below about 600°C, is correct.

With regard to the Chang reference, the disclosure recites the formation of "a gate stack 32, comprising [a] patterned polysilicon layer 30 and [a] patterned metal layer 28, as opposed to a conventional gate stack, which also includes an overlying oxide layer." *See, Chang reference* at col. 3, lines 4-8. A dielectric cap layer is not formed in the process of the Chang reference. Furthermore, the Chang reference does not disclose any teaching or suggestion regarding the temperature at which a dielectric cap layer is disposed or formed over a metallic silicide film. That the Chang reference is void of any teaching or suggestion regarding a method of depositing a dielectric cap layer at a temperature below about 600°C is acknowledged by the Examiner at page 4, ¶ 2 of the outstanding Office Action.

In an effort to supply the teachings missing from the Segawa and Chang references and arrive at that which is claimed in the present application, the Examiner attempts to modify the teachings of the Segawa and Chang references with those of the Possin reference. The Possin reference discloses a method for passivating the back channel regions in amorphous silicon field effect transistors (FETs), particularly those employed in matrix addressed liquid crystal displays. *Possin reference* at col. 2, lines 9-12. "Amorphous silicon FETs typically employed in matrix addressed liquid crystal displays employ a structure in which a portion of the amorphous silicon material is exposed through a metal contact layer." *Id.* at col. 1, lines 41-44. In order to prevent a net positive charge state from being produced on the exposed silicon surface, and thus inducing an electron channel near the surface region causing so-called "back channel leakage," the exposed silicon surface must be protected from environmental contamination. *Id.* at col. 1, lines 54-63. Thus, the Possin reference "is directed to a method for providing a desired degree of protection" from such back channel leakage. *Id.* In order to provide such protection, following a passivation step, the amorphous silicon is exposed to a basic solution and a permanent passivating cap, or dielectric insulating layer, is provided over the substrate. The dielectric insulating layer is preferably deposited by plasma chemical vapor deposition at a temperature of approximately 150°C. *Id.*, col. 4, lines 6-17.

Applicants respectfully submit that there is no suggestion or motivation in the cited references, or from the knowledge generally available in the prior art, which would lead one of ordinary skill in the art to modify the Segawa and Chang references with the teachings of the Possin reference as asserted in the outstanding Office Action. It is stated in the Office Action that "[i]t is the Examiner's position that a person having ordinary skill in the art would have found it obvious to modify [the] Segawa and Chang [references] with the method of depositing a dielectric cap layer below 600°C as taught by [the] Possin [reference] in order to effectively deposit the silicon nitride layer by plasma chemical vapor deposition". Applicants respectfully submit, however, that there is no teaching or suggestion in the Segawa reference that under the disclosed reaction chamber process parameters, the silicon-rich dielectric layer could not be adequately deposited by plasma chemical vapor deposition. On the contrary, in the method of the Segawa reference, the silicon-rich dielectric layer is deposited, under the disclosed reaction chamber process parameters, "by means of a CVD process". *Segawa reference* at col. 7, lines 23-24; col. 7, lines 26-37. *See also*, claim 15 of the present application.

Further, as previously stated, the device produced by the method of the Possin reference is a device wherein exposed amorphous silicon is covered by a dielectric insulating layer to protect the silicon from environmental contamination and thus prevent back channel leakage. *See, Possin reference* at col. 1, lines 54-63. On the other hand, the silicon-rich dielectric cap of the Segawa reference is formed on the surface of a metallic silicide film, not on amorphous silicon. *See, Segawa reference* at col. 7, lines 20-24. Thus, one of ordinary skill in the art would not have been motivated to modify the Segawa reference with the method of protecting exposed amorphous silicon from environmental contamination disclosed by the Possin reference as the dielectric cap of the Segawa reference is not formed on amorphous silicon. Accordingly, there is no teaching or suggestion in the Segawa reference, the Possin reference, or in the prior art, which would lead one skilled in the art to modify the teachings of the Segawa reference with those of the Possin reference as asserted.

Accordingly, Applicants respectfully submit that there would be no motivation for the present combination of the Segawa reference, the Chang reference and the Possin reference as asserted in the outstanding Office Action. "Before the PTO may combine the disclosures of two

or more prior art references in order to establish *prima facie* obviousness, **there must be some suggestion for doing so . . .**" *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598-99 (Fed. Cir. 1998)(emphasis added). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127 (Fed. Cir. 1984). Absent some suggestion to make the asserted modification, it is respectfully submitted that the Examiner has used impermissible "hindsight" occasioned by the Applicants' teachings to hunt through the prior art for the claimed elements and combine them as claimed. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). It is respectfully submitted that such is not an appropriate basis for determining patentability.

Further, as previously stated, the temperature used during the formation of the dielectric cap over the metallic silicide film in each of the embodiments disclosed in the Segawa reference exceeds 600°C. This specific reaction chamber process parameter results in deposition of a layer of material having a silicon-to-other element ratio which exceeds that of the stoichiometric composition of the material deposited. *See, Segawa reference* at col. 7, lines 39-48 (Example I); col. 9, lines 6-18 (Example II); col. 10, lines 5-14 (Example III); col. 11, lines 3-17 (Example IV); col. 11, line 65 – col. 12, line 4 (Example V); col. 12, lines 58-66 (Example VI); col. 13, lines 51-64 (Example VII); col. 14, lines 40-52 (Example VIII). The presence of a dielectric cap having this silicon-to-other element ratio is desired as it improves adhesion between the metallic silicide film and the dielectric cap and decreases the likelihood of peeling during a subsequent heat treatment. *See id.* at col. 7, line 62 – col. 8, line 16.

It is respectfully submitted that there is no teaching or suggestion in either the Possin reference or the Segawa reference, nor is any evidence cited by the Examiner, which would indicate that such a silicon-to-other element ratio may be achieved at the deposition temperature disclosed by the Possin reference, *i.e.*, at about 150°C. Clearly this temperature is well below that disclosed as a desired reaction chamber process parameter by the Segawa reference. There is no teaching or suggestion in the references, or in the prior art, which would indicate a reasonable expectation of success if the Segawa reference was modified with the method of the

Possin reference in the manner asserted. Accordingly, a *prima facie* case of obviousness is precluded. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In view of the foregoing, Applicants respectfully submit that the cited references fail to establish a *prima facie* case of obviousness of claims 3, 17 and 19. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 103(a) of claims 3, 17 and 19 based upon the asserted combination of the Segawa, Chang and Possin references be withdrawn. Claims 3, 17 and 19 are believed to be in condition for allowance and such favorable action is respectfully requested.

Each of the dependent claims of the present invention is also believed to be in condition for allowance because the independent claims from which they depend are in condition for allowance. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (dependent clams are nonobvious under 35 U.S.C. § 103 if the independent claims from which they depend are nonobvious). Thus, it is respectfully requested that the obviousness rejection of claims 4 through 16, 18 and 20 through 22 be withdrawn as well.

Claims 4, 5, 20 and 21 are also independently believed to be in condition for allowance over the asserted combination of references as the Segawa reference, the Chang reference and the Possin reference, whether taken alone or in combination, fail to teach or suggest the formation of a dielectric cap over metallic silicide film within the claimed temperature limitations. More specifically, dependent claims 4 and 20 recite the formation of a dielectric cap layer over a metallic silicide film effected at temperature of between 400°C and 600°C and dependent claims 5 and 21 recite the formation of a dielectric cap over a metallic silicide film effected at a temperature of about 500°C. As previously stated, the Segawa reference discloses formation of a dielectric cap at temperatures in excess of 600°C, the Possin reference discloses formation of a dielectric cap at a temperature of about 150°C and the Chang reference fails to teach or suggest deposition of a dielectric cap at all. As such, the cited references fail to teach or suggest all of the claim limitations and a *prima facie* case of obviousness with respect to these claims is precluded. *See, In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Each of claims 3 through 22 is believed to be in condition for allowance and such favorable action is respectfully requested.

CONCLUSION

Claims 3 through 22 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,

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TLW/ah
Enclosures: Petition for One-Month Extension of Time
Check No. 18652 in the amount of $110.00

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